Jameco Part number 128055

National Semiconductor Corporation

116100 & 128055

ADC0831/ADC0832/ADC0834 and ADC0838
8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or µPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

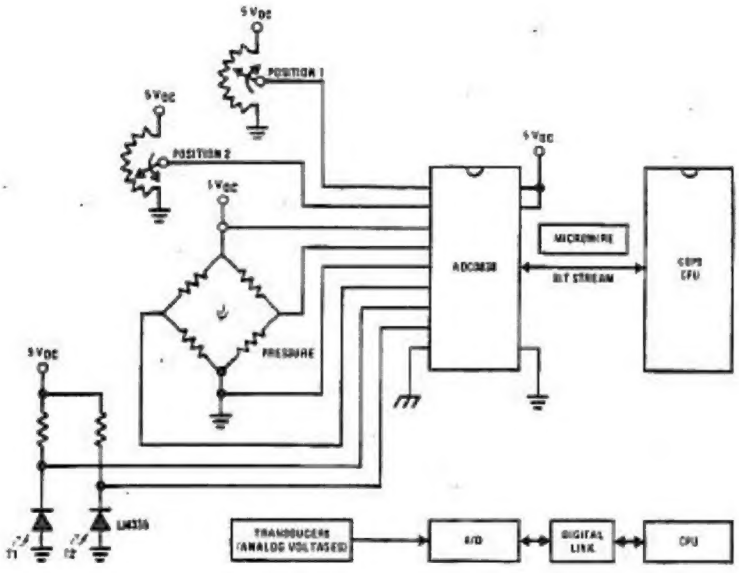
Features

- NSC MICROWIRE compatible–direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3" standard width, 8-, 14- or 20-pin DIP package
- 20 Pin Molded Chip Carrier Package (ADC0838 only)

Key Specifications

■ Resolution	8. Bits
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	32 µs

Typical Application



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, Contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{DC} (Note 3)	6.5V
Voltage	
Logic Inputs	- 0.3V to V_{CC} + 0.3V
Analog Inputs	- 0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	± 5 mA
Package	± 20 mA
Storage Temperature	-65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 5)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0831/2/4/8BJ	-55°C to + 125°C
ADC0831/2/4/8BJ	
ADC0831/2/4/8BCJ	- 40°C to + 85°C
ADC0831/2/4/8CCJ	
ADC0831/2/4/8BCN	-0°C to + 70°C
ADC0838BCV	
ADC0831/2/4/8CCN	
ADC0838CCV	

Converter and Multiplexer Electrical Characteristics

The following specifications apply for V_{CC} = V + = V_{REF} = 5V, $V_{REF} \leq V_{CC}$ + 0.1V, $T_A = T_j$ = 25°C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BJ, CJ, BCJ and CCJ Devices			BCV, CCV, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error	V_{REF} = 5.00 V							
ADC0838BCV	(Note 6)					± ½	± ½	
ADC0831/2/4/8BCN							± ½	LSB
ADC0831/2/4/8BJ			± ½			± ½		
ADC0831/2/4/8BCj			± ½					
ADC0838CCV						± 1	± 1	
ADC0831/2/4/8CCN						± 1	± 1	
ADC0831/2/4/8CJ			**± 1**					
ADC0831/2/4/8CCJ			**± 1**					
Minimum Reference Input Resistance (Note 7)		3.5	**1.3**		3.5	1.3	**1.3**	kΩ
Maximum Reference Input Resistance (Note 7)		3.5	**5.9**		3.5	5.4	**5.9**	kΩ
Maximum Common-Mode Input Range (Note 8)			**V_{CC} + 0.05**			V_{CC} + 0.05	**V_{CC} + 0.05**	V
Minimum Common-Mode Input Range (Note 8)			**GND - 0.05**			GND - 0.05	**GND - 0.05**	V
DC Common-Mode Error		± 1/16	± ¼		± 1/16	± ¼	± ¼	LSB
Change in zero error from V_{CC} = 5V to internal zener operation (Note 3)	15 mA into V + V_{CC} = N.C. V_{REF} = 5V		**1**			1	**1**	LSB
V_Z, internal diode breakdown (at V_+) (Note 3) MIN	15 mA into V +		**6.3**			6.3	**6.3**	V
MAX			**8.5**			8.5	**8.5**	
Power Supply Sensitivity	V_{CC} = 5V ± 5%	± 1/16	± ¼	± ¼	± 1/16	± ¼	± ¼	LSB

Converter and Multiplexer Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = V+ = 5V, $T_A = T_I = 25°C$, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BJ, CJ, BCJ and CCJ Devices			BCV, CCV, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)								
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel=5V Off Channel=0V		**-0.1**	**-1**		-0.2	**-1**	ìA
	On Channel=0V Off Channel=5V		**+0.1**	**+1**		+0.2	**+1**	ìA
I_{ON} On Channel Leakage Current (Note 9)	On Channel=0V Off Channel=5V		**-0.1**	**-1**		-0.2	**-1**	ìA
	On Channel=5V Off Channel=0V		**+0.1**	**+1**		+0.2	**+1**	ìA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC}=5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC}=4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN}=5.0V	0.005	**1**		0.005	1	**1**	ìA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN}=0V	-0.005	**-1**		-0.005	-1	**-1**	ìA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC}=4.75V I_{OUT}=-360 ìA		**2.4**			2.4	**2.4**	V
	I_{OUT}=-10 ìA		**4.5**			4.5	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC}=4.75V I_{OUT}=1.6 mA		**0.4**			0.4	**4.0**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT}=0V	-0.1	**-3**		-0.1	-3	**-3**	ìA
	V_{OUT}=5V	0.1	**3**		0.1	+3	**-3**	ìA
I_{SOURCE}, Output Source Current (Min)	V_{OUT}=0V	-14	**-6.5**		-14	-7.5	**-6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT}=VCC	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max) ADC0831, ADC0834, ADC0838		0.9	**2.5**		0.9	2.5	**2.5**	mA
ADC0832	Includes Ladder Current	2.3	**6.5**		2.3	6.5	**6.5**	mA

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AC Characteristics

The following specifications apply for V_{CC} = 5V, $t_f = t_f$ = 20 ns and 25°C unless otherwise specified.

Parameter	Conditions	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Limit Units
Min f_{CLK}, Clock Frequency			10		kHz
Max				400	kHz
t_C, Conversion Time	Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle Min				40	%
(Note 10) Max				60	%
t_{SET-UP} CS Falling Edge or Data Input Valid to CLK Rising Edge				250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge				90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 11)	C_L=100 pF				
	Data MSB First	650		1500	ns
	Data LSB First	250		600	ns
t_{1H}, t_{0H},--Rising Edge of CS to Data Output and SARS Hi-Z	C_1 = 10 pF, R_L = 10k (see TRI-STATE(ER) Test Circuits)	125		250	ns
	C_t=100 pf, R_L=2k		500		ns
C_{IN}, Capacitance of Logic Input		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground plugs.

Note 3: Internal zener diodes (8.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V-. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+ (*See Figure 3* in Functional Description Section 6.0)

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < V- or V_{IN} > V+) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Note 7: Cannot be tested for ADC0832.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct--especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{CC} to 5 V_{CC} input voltage range will therefore require a minimum supply voltage of 4.95 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 µs. The maximum time the clock can be high is 60 µs. The clock can be stopped when low so long as the analog input voltage remains stable.

Note 11: Since data. MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Note 12: Typicals are at 25°C and represent most likely parametric horm.

Note 13: Tested limits are guaranted to National's AOQL (Average Outgoing Quality Level).

Note 14: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

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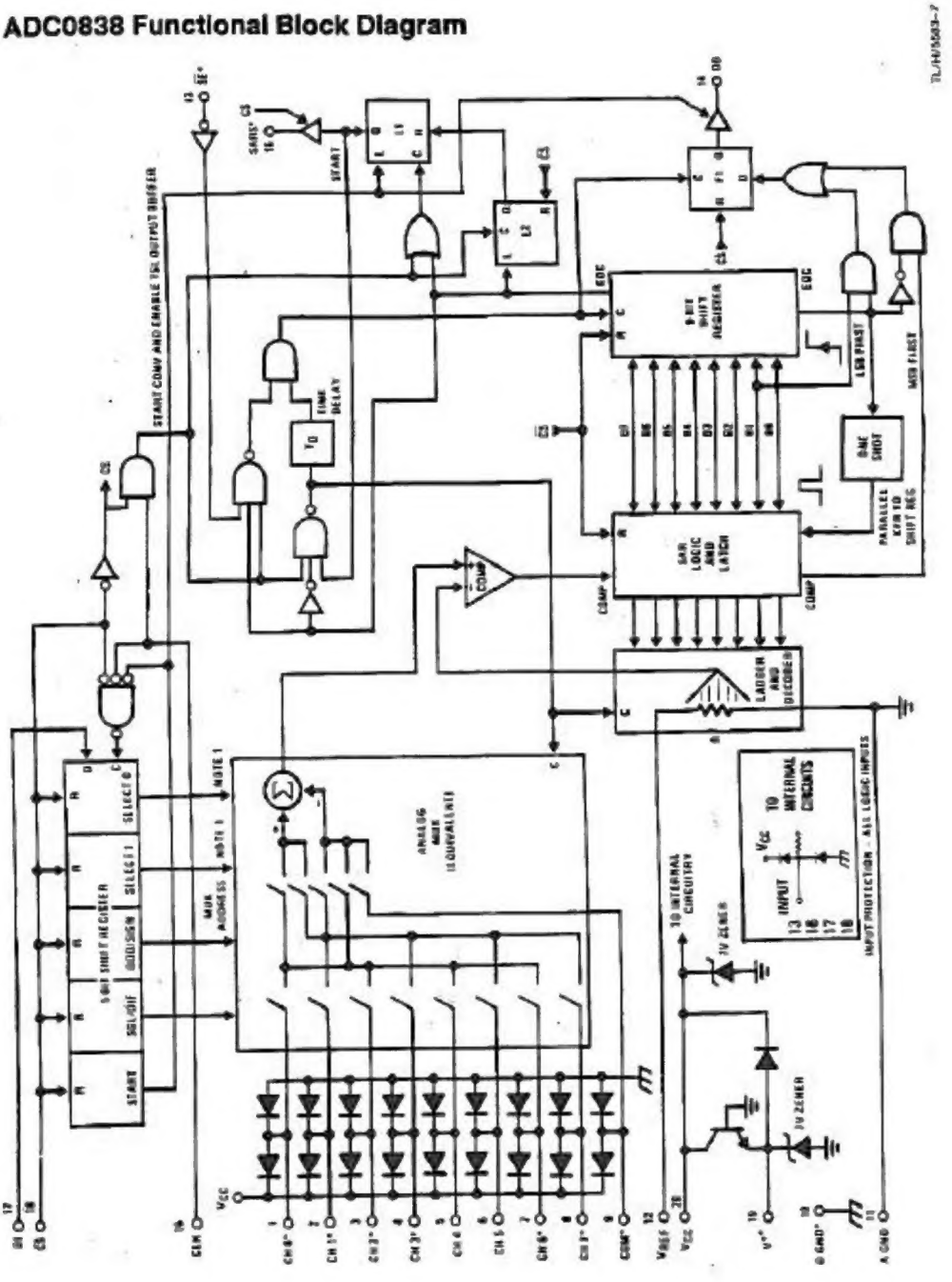
ADC0838 Functional Block Diagram



* Some of these functions/pins are not available with other options.

Note 1: For the ADC0834, D1 is input directly to the D input of SELECT 1. SELECT 0 is forced to a "1". For the ADC0832, D1 is input directly to the D1 input of ODD/SIGN, SELECT 0 is forced to a "0" and SELECT 1 is forced to a "1".

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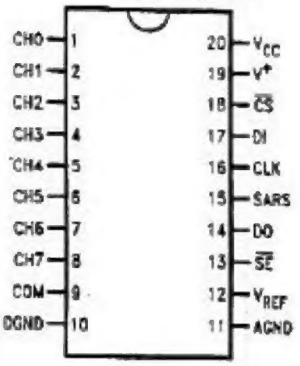
Connection Diagrams

ADC0838 8-Channel MUX

Dual-In-Line Package



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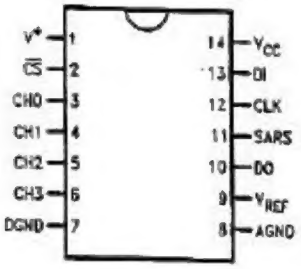
Top View

ADC0834 4-Channel MUX

Dual-In-Line Package



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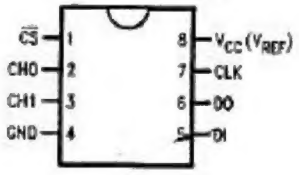
Top View

COM internally connected to A GND

ADC0832 2-Channel MUX

Dual-In-Line Package



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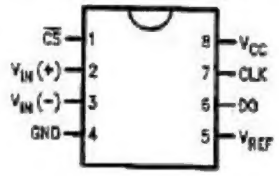
Top View

COM internally connected to GND.

V_{REF} internally connected to V_{CC}.

ADC0831 Single Differential Input

Dual-In-Line Package



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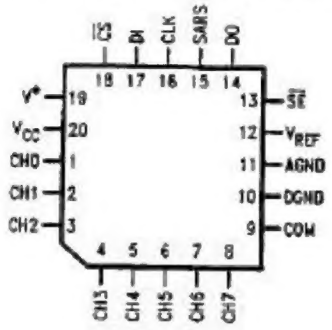
Top View

ADC0838 8-Channel MUX

Molded Chip Carrier (PCC) Package



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